Amendments to the Claims:

1. (Currently amended) An integrated circuit comprising:

a bondable metal pad defined on a stress-buffering dielectric layer;

a damascened intermediate metal layer fabricated in a first inter-metal dielectric (IMD) layer that is under said stress-buffering dielectric layer, and said damascened intermediate metal layer being disposed directly under said bondable metal pad and electrically connected to said bondable metal pad through a plurality of via plugs integrated with said bondable metal pad;

at least one electrically isolated damascened metal frame fabricated in a second IMD layer under said first IMD layer, said damascened metal frame, having four sides and dimensions corresponding to peripheral contour of overlying said intermediate metal layer exhibits ability in counteracting mechanical stress exerted on said bondable metal pad during bonding, being disposed directly under said damascened intermediate metal layer; and

a portions of active circuit components of said integrated circuit disposed directly under said damascened metal frame.

2. (Original) The integrated circuit according to claim 1 wherein said stress-buffering dielectric layer is structurally denser than any of said first IMD layer and second IMD layer.

3. (Original) The integrated circuit according to claim 2 wherein said stress-buffering dielectric layer is made of silicon dioxide.

4. (Original) The integrated circuit according to claim 1 wherein said stress-buffering dielectric layer and a peripheral area of said bondable metal pad is covered by a passivation layer.

5. (Original) The integrated circuit according to claim 4 wherein said passivation layer is made of silicon nitride.

6. (Original) The integrated circuit according to claim 4 wherein said passivation layer is made of polyimide.

7. (Original) The integrated circuit according to claim 4 wherein said passivation layer has a window exposing a top surface area of said bondable metal pad.

8. (Original) The integrated circuit according to claim 1 wherein said damascened intermediate metal layer comprises copper conductor core and a diffusion barrier layer disposed between said copper conductor core and said first IMD layer.

9. (Original) The integrated circuit according to claim 1 wherein said bondable metal pad comprises aluminum.

10. (Original) The integrated circuit according to claim 1 wherein said plural via plugs are made of aluminum.

11. (Original) The integrated circuit according to claim 1 wherein said damascened metal frame comprises copper.

12. (Currently amended) An integrated circuit comprising:

an aluminum bonding pad defined on a stress-buffering dielectric layer;

an aluminum active circuit layout, wherein said aluminum active circuit layout and said aluminum bonding pad are simultaneously defined on said stress-buffering dielectric layer;

a damascened intermediate copper layer fabricated in a first inter-metal dielectric

(IMD) layer that is under said stress-buffering dielectric layer, and said damascened intermediate copper layer being disposed directly under said aluminum bonding pad and electrically connected to said aluminum bonding pad through a plurality of via plugs integrated with said aluminum bonding pad;

~~at least one~~ an electrically isolated first damascened copper frame fabricated in a second IMD layer under said first IMD layer, said damascened copper frame, having four sides and dimensions corresponding to peripheral contour of overlying said intermediate metal layer exhibits ability in counteracting mechanical stress exerted on said bondable metal pad during bonding, being disposed directly under said damascened intermediate copper layer; ~~and~~

an electrically isolated second damascened copper frame encompassed by said first damascened copper frame; and

a portions of active circuit components of said integrated circuit disposed directly under said first and second damascened metal frame.

13. (Original) The integrated circuit according to claim 12 wherein said stress-buffering dielectric layer is structurally denser than any of said first IMD layer and second IMD layer.

14. (Original) The integrated circuit according to claim 13 wherein said stress-buffering dielectric layer is made of silicon dioxide.

15. (Original) The integrated circuit according to claim 12 wherein said stress-buffering dielectric layer, said aluminum active circuit layout over said stress-buffering dielectric layer, and a peripheral portions of said aluminum bonding pad are covered by a passivation layer.

16. (Original) The integrated circuit according to claim 15 wherein said passivaiton layer

is made of polyimide.